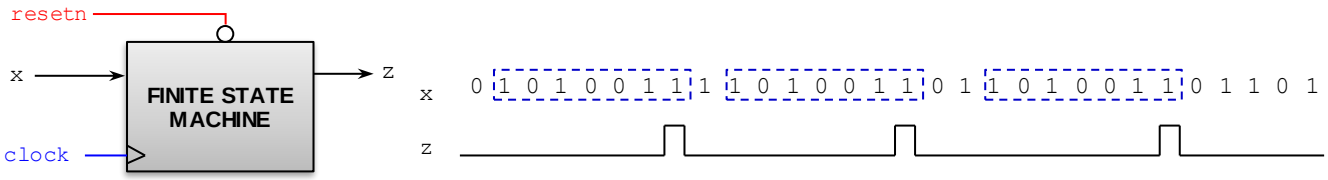
Homework 4

(Due date: March 28th @ 5:30 pm)
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (23 PTS)

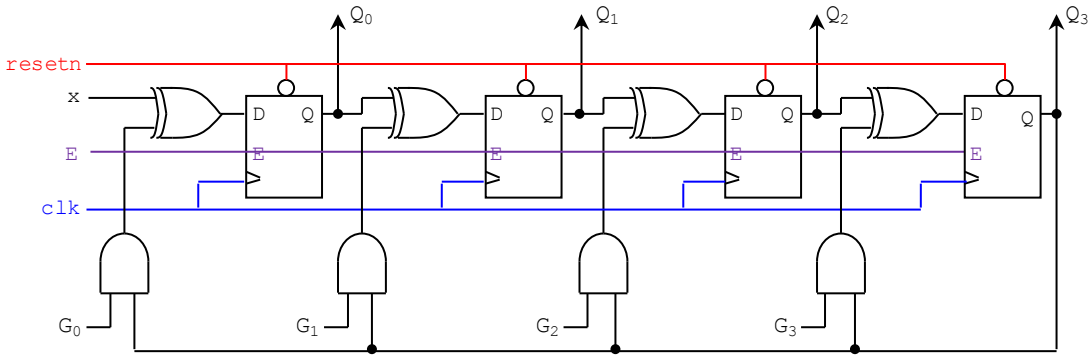
- Sequence Detector: The machine has to generate z=1 when it detects the sequence 1010011. Once the sequence is detected, the circuit looks for a new sequence.

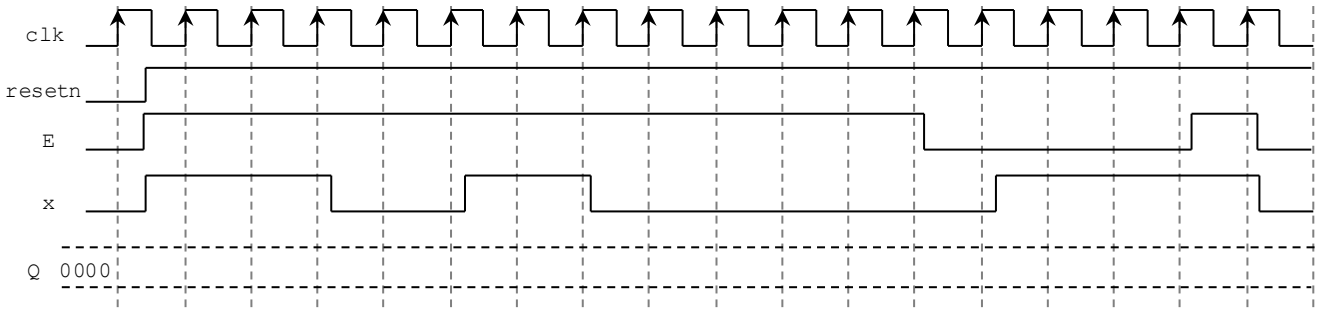


- Draw the State Diagram (any representation), State Table, and Excitation Table. Is this a Mealy or a Moore machine? Why?
- Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (5 pts)
- Sketch the circuit. (3 pts)

PROBLEM 2 (15 PTS)

- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 1001$, $Q = Q_3Q_2Q_1Q_0$

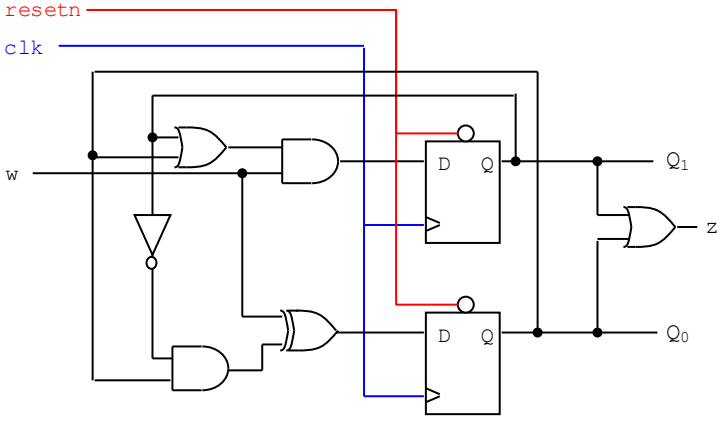




PROBLEM 3 (12 PTS)

- Provide the State Diagram (any representation), the Excitation Table, and the Excitation equations of the following FSM.

  w: input, z: output, Q_1Q_0: state.

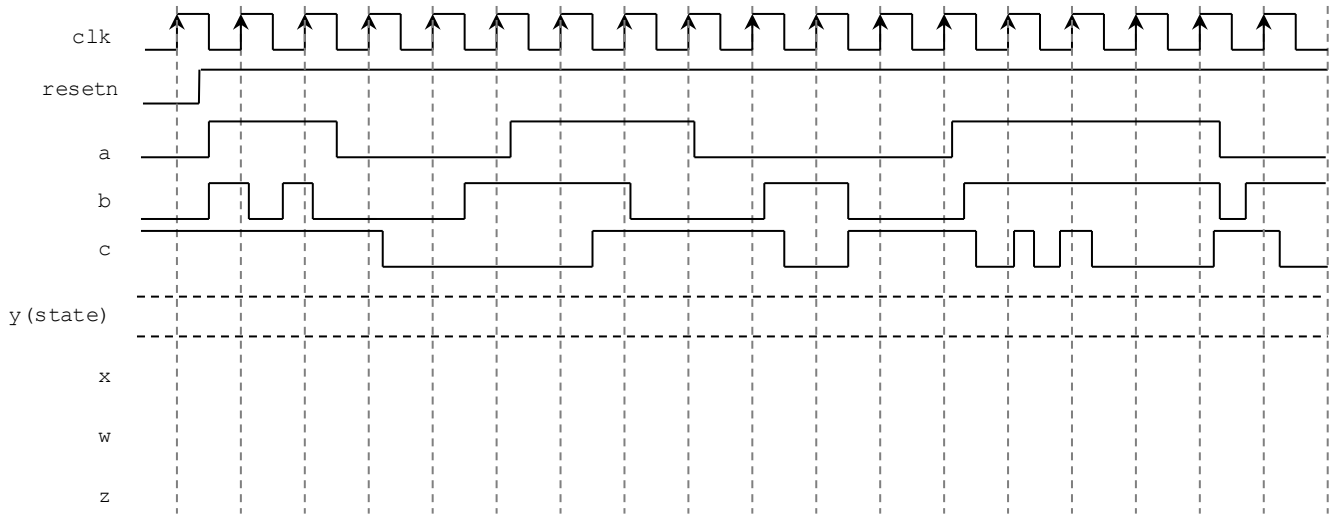


PROBLEM 4 (17 PTS)

- Draw the State Diagram (in ASM form) of the FSM whose VHDL description in shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

```
library ieee;
use ieee.std_logic_1164.all;

entity myfsm is
   port ( clk, resetn: in std_logic;
          a, b, c: in std_logic;
          x, w, z: out std_logic);
end myfsm;
```

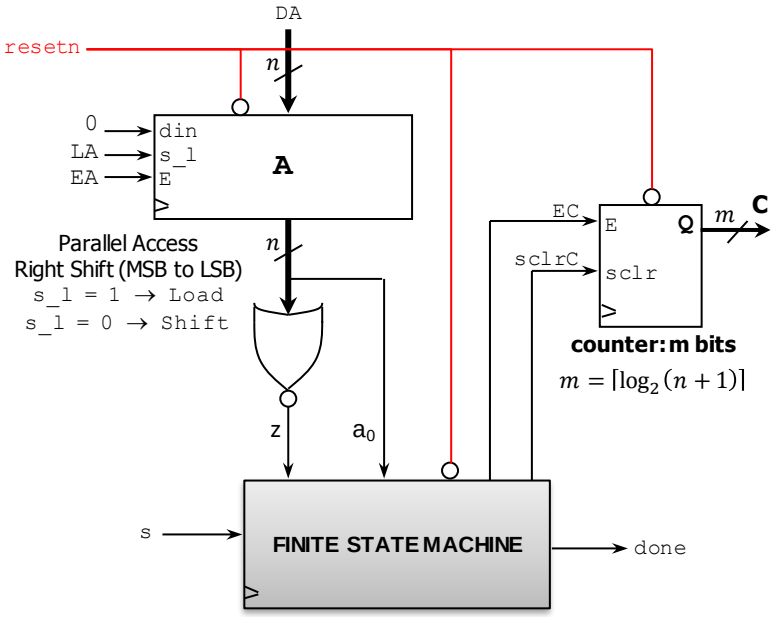
```
architecture behavior of myfsm is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, a, b, c)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if a = '1' then
               y <= S2;
            else
               if b = '1' then y <= S3; else y <= S1; end if;
            end if;

          when S2 =>
            if b = '1' then y <= S1; else y <= S3; end if;

          when S3 =>
            if c = '1' then y <= S3; else y <= S2; end if;

        end case;
     end if;
  end process;

  Outputs: process (y, a, b, c)
  begin
      x <= '0'; w <= '0'; z <= '0';
      case y is
         when S1 => if a = '0' then
                       if b = '0' then
                          z <= '1'; x <= '1';
                       end if;
                    end if;

         when S2 => if c = '0' then x <= '1'; end if;
                    if b = '0' then w <= '1'; end if;

         when S3 => if c = '0' then x <= '1'; end if;
      end case;
  end process;
end behavior;
```

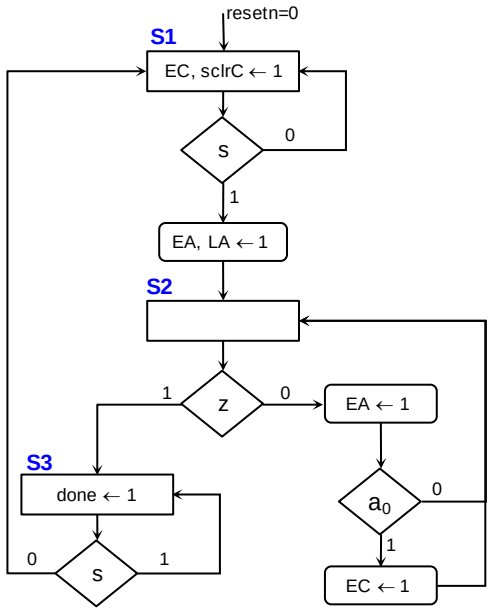


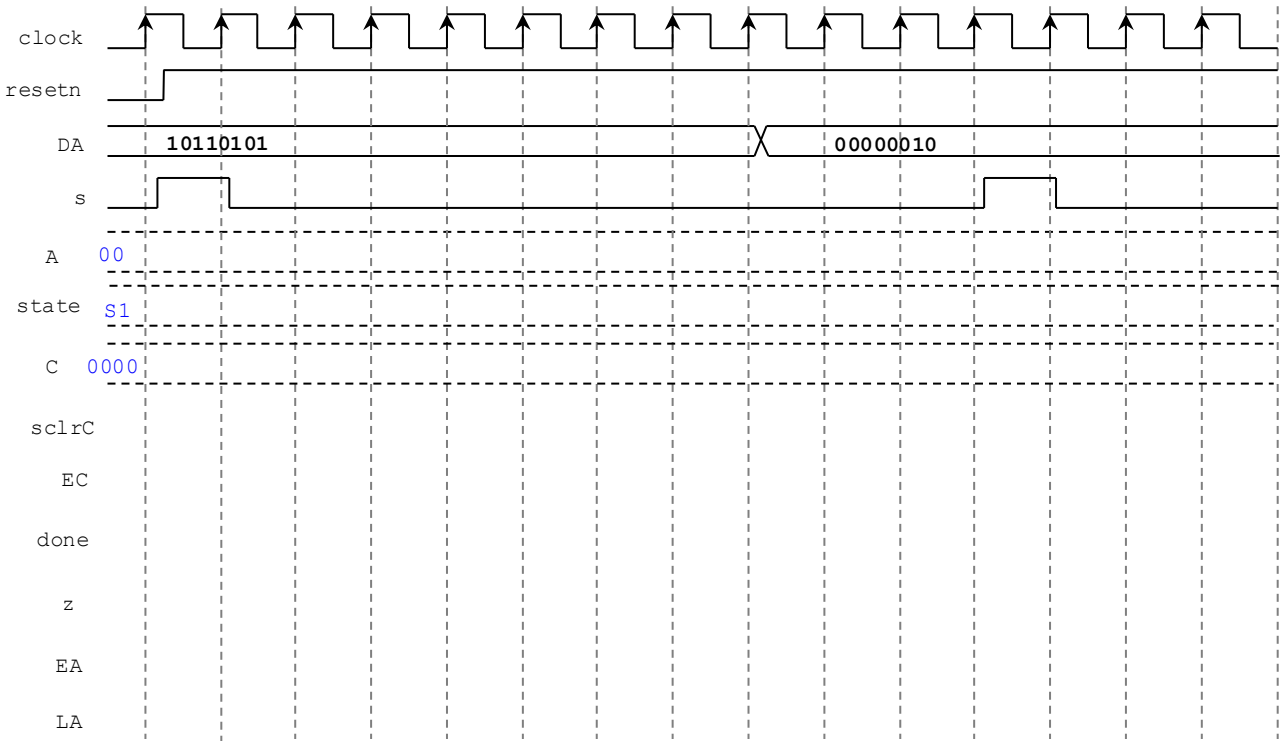
PROBLEM 5 (18 PTS)

- "Counting 1's" Circuit: It counts the number of bits in register A that has the value of '1'. The digital system is depicted below: FSM + Datapath. Example: For $n = 8$: if $A = 00110110$, then $C = 0100$.
  - ✓ m-bit counter: If $E = sclr = 1$, the count is initialized to zero. If $E = 1, sclr = 0$, the count is increased by 1.
  - ✓ Parallel access shift register: If $E = 1$: $s\_l = 1 \rightarrow$ Load, $s\_l = 0 \rightarrow$ Shift.
- Complete the timing diagram where $n = 8, m = 4$.

```
C ← 0
while A ≠ 0
   if a0 = 1 then
      C ← C + 1
   end if
   right shift A
end while
```







PROBLEM 6 (15 PTS)

- Attach a printout of your Project Status Report (no more than a page). This report should contain the current status of the project, including a block diagram of your system. You **MUST** use the provided template (`Final Project - Report Template.docx`).